

[0001] TITLE: Low-Power High-Speed 4-2 Compressor with
Minimized Transistor Count

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[0003] **BACKGROUND OF THE INVENTION**

[0004] FIELD OF THE INVENTION

This invention relates to an XOR/XNOR cell, and particularly to a new full adder
employing XOR/XNOR cells and a 4-2 compressor design having the full adder circuit.

[0005] DESCRIPTION OF BACKGROUND

[0006] Before the claimed invention in a private and new
development Messrs Radhakrishnan and Bayoumi created a new
design for an XOR/XNOR cell which was a minimum sized cell
and which was then the subject of an investigation during my
work at IBM.

[0007] SUMMARY OF THE INVENTION

[0008] As a result of the investigation of the cell shown in Figure 1, a new form of a high-speed, low-power, reduced transistor count, 4-2 compressor was created. This investigation led to the described Full Adder improvements which include now preferably the XOR/XNOR cell circuit and to the preferred embodiment of a 4-2 compressor circuit having as an element of the design dual XOR/XNOR cells in the 4-2 compressor circuit.

[0009] This unit is a common component in VLSI multipliers can be used for the reduction of partial products. Since multiplication is one of the most used and power hungry operations of DSPs and specialized microprocessors, it is quite evident that a reduction in the power consumption of multipliers is a great resource for improving the overall performance of the processor. This could be used in many levels of technology, such as:

[0010] - Reducing the power consumption, and hence, the heat dissipation of large scale parallel processor modules.

[0011] - Extending the battery life (and/or possibly expanding the processing power) of portable pervasive computing devices.

[0012] - Since partial product reduction is responsible for much of the delay of multiplication, the new compressor may help to increase the performance of many microprocessor/DSP systems.

[0013] As a result of the investigation of the cell shown in Figure 1, a new form of a high-speed, low-power, reduced transistor count, 4-2 compressor was created. This unit is a common component in VLSI multipliers can be used for the reduction of partial products. Since multiplication is one of the most used and power hungry operations of DSPs and specialized microprocessors, it is quite evident that a reduction in the power consumption of multipliers is a great resource for improving the overall performance of the processor. This could be used in many levels of technology, such as:

[0014] Reducing the power consumption, and hence, the heat dissipation of large scale parallel processor modules.

[0015] Extending the battery life (and/or possibly expanding the processing power) of portable pervasive computing devices.

[0016] Since partial product reduction is responsible for much of the delay of multiplication, the new compressor may help to increase the performance of many microprocessor/DSP systems.

[0017] Additional advantages may be realized with the 4-2 compressor design of the present invention. Other embodiments and aspects of the invention which may be developed from the circuits described in detail herein and are considered a part of the

claimed invention. For a better understanding of the invention with advantages and features, refer to the description and to the drawings.

[0018] BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0020] FIG. 1 illustrates the new XOR/XNOR cell used in the investigation as a Damu XOR/XNOR cell ($H = A \text{ xor } B$, $H' = A \text{ xnor } B$).

[0021] FIG. 2 illustrates the preferred embodiment of the invention having a Full adder using minimum sized XOR/XNOR cells and a 2-1 MUX circuit.

[0022] Figure 3 shows truth tables in Figures 3A-3D.

[0023] Figure 4 illustrates the complete 4-2 compressor design of the preferred embodiment.

[0024] The detailed description explains the preferred embodiments of the invention, together with advantages and features, by way of example with reference to the drawings.

[0025] DETAILED DESCRIPTION OF THE INVENTION

[0026] This invention was created after an investigation of full adders which are often used in creating 4-2 compressors with a new adder. The adder that was used in the investigation was, in fact, a new design was created using the minimum sized XOR/XNOR cell developed but not published by Messrs Radhakrishnan and Bayoumi. The XOR/XNOR cell used in the investigation can be seen in Figure 1. It is an improvement on this cell that will be described.

[0027] By replicating the XOR/XNOR cell twice as shown in Figure 2 it will be seen that the sum of the Full Adder (FA) was created. Inclusion of a simple 2-1 MUX is used for the generation of a Cout signal. Accordingly, Figure 2 illustrates our preferred Full adder using minimum sized XOR/XNOR cells and a 2-1 MUX in the circuit for the new 4-2 compressor. It is a feature of this new circuit that a new complementary sum signal is produced.

[0028] Figures 3A through 3D develop the truth table for the Full Adder design of the preferred embodiment. Figure 3A shows a new 4-2 compressor truth table. Figure 3B shows the 'Sum' output divided into two sections controlled by the XOR/XNOR of the two MSBs of the inputs. Cout is configured such that it is a repetitive pattern in each quarter. Figure 3C: illustrates the commonalities between Carry and 'Sum, 0, or 1' controlled by XOR/XNOR of 2 MSBs of inputs. Finally, Figure 3D shows the minimized table with reference to new Full Adder design.

[0029] The significance of the new 4-2 compressor developed with the full adder design can now be understood by observing a 4-2 compressor truth table as shown in Figure 3a. This table was created by modifying the output signals to conform to some specific patterns as shown in Figures 3b and 3c. This entire table, once created can be simplified to a very basic table with reference to the Full Adder mentioned earlier and described with respect to Figure 2. This can be seen in the minimized table of Figure 3d.

[0030] Figure 4 illustrates the circuit for use in a microprocessor in accordance with the preferred embodiment showing a complete 4-2 compressor design of the preferred embodiment.

[0031] Many others have investigated areas of concern with respect to power consumption in VLSI. Some have worked on new designs for XOR/XNOR, Full Adder, and 4-2 compressor designs. This new design has taken a single minimized XOR/XNOR cell and created a completely new 4-2 compressor. This compressor is also created using a new Full Adder circuit that was also created using the high-speed low-power XOR/XNOR cells. Other 4-2 compressor designs have improved the speed or the power consumption or the size of current designs. This new circuit improves all three of these parameters. By using the XOR/XNOR circuits, improvements are made in both speed and power consumption. And the new design has an overall transistor count of 30 which is equal to some of the smallest 4-2 compressor designs to date.

[0032] The speed and power characteristics can also be adjusted by using other XOR/XNOR cells in place of the one shown herein by those of ordinary skill in the art.

[0033] While the preferred embodiment to the invention has been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

Figure 1 shows the construction of the full adder circuit with complementary sum which was designed using two of the XOR/XNOR circuits described in Damu Radhakrishnan's paper. The full circuit is comprised bits A and B passed into Damu's (1) XOR/XNOR circuit wherein, the XOR of this unit, along with the carry in bit, are passed into another (2) XOR/XNOR circuit. The outputs of this circuit are (3) a fully-recoverable (to Vdd) Sum and (4) complementary Sum (Sum') of A, B, and Cin. The Cout of the adder is created by passing the Cin and A bits into a (5) pass-logic 2-1 multiplexer.

Figure 4 shows the completed 4-2 compressor as a 'gray box' design. The complete design is created using: (1) one of the new Full Adder circuits, (2) another instance of the XOR/XNOR cell, and (3,4) two pass-logic 2-1 multiplexers. These cells are connected by having input bits X, Y, and Z passed into the full adder, which generates (5) the first order carry out [Cout], (6) intermediate sum [S], and (7) intermediate complementary sum [S']. The last input bits, W and Cin, are passed into the second XOR/XNOR circuit, generating (8) the intermediate XOR signal [I] and (9) the intermediate XNOR signal [I']. The complementary sum [S'] and the intermediate sum [S] are passed into one of the 2-1 MUXs using the intermediate XOR signal [I] as the control. The output of this MUX is

[10] the final sum [SUM]. The complementary sum [S'] and the carry-in bit [Cin] are passed into the final 2-1 MUX. By using the intermediate XNOR as the control signal, the [11] second order carry out [Carry] is generated.